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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,745	09/30/2003	Manu Gulati	BP3252	8011

51472 7590 12/17/2008

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EXAMINER	
AHMED, SALMAN	
ART UNIT	PAPER NUMBER
2419	
MAIL DATE	DELIVERY MODE
12/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,745	GULATI ET AL.	
	Examiner	Art Unit	
	SALMAN AHMED	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/12/2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8-12,14,15 and 17-29* is/are rejected.

7)☒ Claim(s) *3,4,6,7,13 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-29 are pending.

Claims 1, 2, 5, 6, 8-12, 14, 15 and 17-29 are rejected.

Claims 3, 4, 6, 7, 13 and 16 are objected to.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 5, 6, 8-12, 14, 15 and 17-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Oberman et al., hereinafter Oberman, (US7042891).

Regarding claim 1, Oberman discloses dynmic selection of lowest latency path in a network switch (see Oberman col. 2 lines 29 - 58) comprising: • receiving a data block at a receiver of the host device (see Oberman col. 2 lines 59-62); • storing the data block in a receiver buffer (see Oberman col. 7 lines 32-35); • determining an input virtual channel corresponding to the data block (see Oberman col. 8 lines 11-15); • updating an input virtual channel linked list corresponding to the input virtual channel to include the data block (see Oberman col. 7 lines 29-57) • determining an output virtual channel for the data block (see Oberman col. 8 lines 11-15); • transferring the data block from the input virtual channel linked list of the receiver buffer to a destination within the host

device via the output virtual channel (see Oberman col. 8 lines 20-33); • updating the input virtual channel linked list to remove the data block (see Oberman col. 9 line 65).

Regarding claim 2, Oberman teaches determining an output virtual channel for the data block includes processing one or more of the input virtual channel, a header corresponding to the data block (see Oberman col. 9 lines 25-67), a protocol corresponding to the data block (see Oberman col. 22 lines 23), source identifier/address corresponding to the data block (see Oberman col. 10 lines 43), and a destination identifier/address corresponding to the data block (see Oberman col. 8 lines 2).

Regarding claims 5 and 14, Oberman teaches comprising writing a data block to the receiver buffer and reading a data block from the receiver buffer in a single read/write cycle (see Oberman col. 11 lines 41-47).

Regarding claims 6 and 15, Oberman teaches further comprising anticipating the write of a data block to the receiver buffer in a subsequent read/write cycle by reading a new free linked list head address from the receiver buffer an old free linked list head address in a current read/write cycle (see Oberman col. 14 lines 52-55).

Regarding claims 8 and 17, Oberman teaches further comprising supporting a plurality of input virtual channel linked lists, wherein each input virtual channel linked list corresponds to a respective input virtual channel (see Oberman col. 9 lines 44-45).

Regarding claims 9 and 19, Oberman teaches further comprising supporting a free linked list that includes a plurality of vacant data blocks of the receiver buffer (see Oberman col. 7 lines 30).

Regarding claim 10, Oberman teaches further comprising maintaining a mapping indicating a relationship between a plurality of input virtual channels and a plurality of output virtual channels (see Oberman col. 8 lines 36-40).

Regarding claim 11, Oberman discloses dynmic selection of lowest latency path in a network switch (see Oberman col. 2 lines 29 - 58) comprising: • receiving a data block at a receiver of the host device (see Oberman col. 2 lines 59-62), the data block received via an input virtual channel (see Oberman col. 8 lines 11-15); • storing the data block in a receiver buffer (see Oberman col. 7 lines 32-35); • when the input virtual channel has identified therewith an output virtual channel updating an output virtual channel linked list corresponding to the output virtual channel to include the data block (see Oberman col. 8 lines 11-15); and • when the input virtual channel has not identified therewith an output virtual channel (see Oberman col. 9 line 25-26): o updating an input virtual channel linked list corresponding to the input virtual channel to include the data block (see Oberman col. 7 lines 29-57); o processing the data block to determine an output virtual channel for the data block (see Oberman col. 9 line 25-26); o updating an output virtual channel linked list corresponding to the output virtual channel to include the data block (see Oberman col. 9 line 25-67); and o updating the input virtual channel linked list to remove the data block (see Oberman col. 9 line 65).

Regarding claim 12, Oberman teaches further comprising: • transferring the data block from the receiver buffer to a destination within the host device based upon a corresponding output virtual channel (see Oberman col. 9 lines 25-65); and

• updating the output virtual channel linked list to remove the data block (see Oberman col. 9 lines 65-67).

Regarding claim 18, Oberman teaches further comprising supporting a plurality of output virtual channel lined lists, wherein each output virtual channel linked list corresponds to a respective output virtual channel (see Oberman col. 23 lines 17-35).

Regarding claim 20, Oberman discloses dynmic selection of lowest latency path in a network switch (see Oberman col. 2 lines 29 - 58) comprising: • an input that receives data blocks corresponding to a plurality of input virtual channels (see Oberman col. 2 lines 59-62); • a routing module that determines an output virtual channel for data blocks based upon their respective input virtual channels (see Oberman col. 8 lines 11-15); • a receiver buffer operable to instantiate an input virtual channel linked list for storing data blocks on an input virtual channel basis and to instantiate a free list that identifies free data locations (see Oberman col. 7 lines 29-57); • a linked list control module (see Oberman figure 1 box 404 cluster link memory) operably coupled to the receiver buffer (see Oberman figure 1 box 402 input FIFO); • free linked list registers (see Oberman figure 1 box 406 packet free queue) operably coupled to the linked list control module (see Oberman figure 1 box 404 cluster link memory).

Regarding claim 21, Oberman teaches further comprising an output athat transmits data blocks corresponding to a plurality of input virtual channels (see Oberman figure 18 and col. 23 lines 17-35 and col. 9 lines 18-64).

Regarding claim 22, Oberman teaches wherein: • the receiver buffer is further operable to instantiate an output virtual channel linked list for storing data blocks on an output virtual channel basis (see Oberman figure 18 ref462 and col. 23 lines 17-35); and • the system further comprises output virtual channel linked list registers operably coupled to the linked list control module (see Oberman figure 18 ref 462) and an input virtual channel to output virtual channel map (see Oberman col. 8 lines 11-15).

Regarding claim 23, Oberman teaches the receiver buffer comprises: • a pointer memory (see Oberman figure 1 box 404 cluster link memory); and • a data memory, wherein a single address addresses corresponding locations of the pointer memory and of the data memory (see Oberman figure 1 box 466 packet link memory).

Regarding claim 24, Oberman teaches the receiver buffer further comprises a packet status memory, wherein a single address addresses corresponding locations of the pointer memory, the data memory (see Calamvokis col. 4 lines 6-14), and the packet status memory (see Oberman figure 1 box 406 packet free queue).

Regarding claim 25, Oberman teaches further comprising a pointer memory read port (see Oberman figure 6 ref 478 sfreadwordptr), a pointer memory write port (see Oberman figure 6 ref 476 writewordptr), a data memory read port (see Oberman col. 8 line 35), and a data memory write port (see Oberman col.8 line 34), each of which can access the receiver buffer in a common read/write cycle (see Oberman col. 7 lines 37-39).

Regarding claim 26, Oberman teaches wherein: a single pointer memory location can be read from and written to in a common read/write cycle (see Oberman col. 11 lines 41-47); and a single data memory location can be read from and written to in a common read/write cycle (see Oberman col. 7 lines 37-39).

Regarding claim 27, Oberman teaches wherein the receiver buffer comprises: • a pointer memory (see Oberman figure 6 ref 478 sfreadwordptr); • a data memory (see Oberman col. 8 lines 34-35); • a packet status memory (see Oberman figure 3 packet descriptor memory); and • wherein a single address addresses corresponding locations of the pointer memory, the data memory, and the packet status memory (see Oberman col. 7 lines 21-28).

Regarding claim 28, Oberman teaches further comprising: • a pointer memory read port (see Oberman figure 6 ref 478 sfreadwordptr); • a pointer memory write port (see Oberman figure 6 ref 476 writewordptr); • a data memory read port (see Oberman col. 8 line 35); • a data memory write port (see Oberman col. 8 line 33); • a packet status memory read port (see Oberman figure 3 free remove/add ptr); and • a packet status memory write port (see Oberman figure 3 free remove/add ptr).

Regarding claim 29, Oberman teaches wherein: • a single pointer memory location can be read from and written to in a common read/write cycle (see Oberman figure 6); • a single data memory location can be read from and written to in a common read/write cycle (see Oberman col. 8 lines 34-35); and • a single packet status memory location can be read from and written to in a common read/write cycle (see Oberman figure 3 free remove/add ptr).

Allowable Subject Matter

1. Claims 3-4, 7, 13, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

1. Applicant's arguments see pages 11-14 of the Remarks section, filed 9/12/2008, with respect to the rejections of the claims have been fully considered and are not persuasive.

Applicant argues (see page 11) that the cluster link memory of Oberman, for example, does not recite updating an input virtual channel linked list corresponding to the input virtual channel to include the data block.

However, Examiner respectfully disagrees with the Applicant's assertion. Oberman does indeed teach the cited limitations. Specifically, Oberman teaches updating an input virtual channel linked list corresponding to the input virtual channel to include the data block (see Oberman col. 7 lines 29-57, Input block 400 may further comprise a cluster link memory 404, a packet free queue 406, and a packet descriptor memory 408. Cluster link memory 404 may be configured as a linked list memory to store incoming packets. Packet free queue 406 is configured to operate as a "free list" to specify which memory locations are available for storing newly received packets. In some embodiments, input block 400 may be configured to allocate storage within shared memory 440 using clusters. In this embodiment, a cell is the minimum number of bytes that can be read from or written to shared memory 440 (e.g., 512 bits or 64

bytes). The cell size is a function of the interface with shared memory 440. However, in some embodiments, a number of cells (e.g., two cells) may be defined as a "cluster". Clusters are used to reduce the number of bits required for tracking and managing packets. Advantageously, by dividing packets into clusters instead of cells, the overhead for each packet may potentially be reduced. For example, in one embodiment shared memory 440 may allocate memory in 128-byte clusters. The cluster size may be selected based on a number of factors, including the size of shared memory 440, the average and maximum packet size, and the size of packet descriptor memory 408. However, the potential disadvantage is that a small packet that would normally fit within a single cell will nevertheless be assigned an entire cluster (i.e., effectively wasting a cell). While this is a design choice, if the number of small packets is low relative to the number of large packets, the savings may outweigh the disadvantages).

Oberman further teaches FIG. 3 illustrating details of one embodiment of the cluster link memory, packet free queue, and packet descriptor memory from FIG. 1; and FIG. 4 illustrating details of one embodiment of the queue descriptor memory and queue link memory from FIG. 1. Oberman teaches in FIG. 3 illustrating details of one embodiment of cell link memory 404, packet free queue 406, and packet descriptor memory 408. As shown in the figure, packet free queue 406 comprises a linked list of pointers to free packet descriptors within packet descriptor memory 408 (interpreted as virtual channel linked list). While different configurations are possible and contemplated, each packet descriptor may comprise a start or head pointer and an end or tail pointer to cluster link memory 404 (interpreted as virtual channel linked list).

Cluster link memory may comprise pointers to different memory locations within shared memory 440. In some embodiments, two free pointers (i.e., a free add pointer and a free remove pointer) may be used to access available locations within packet free queue 406. This causes packet free queue to act as a queue as opposed to a stack. This configuration may advantageously yield lower probability of soft errors occurring in times of low utilization when compared with a configuration that utilizes packet free queue 406 as a stack. FIG. 4 illustrates details of one embodiment of queue descriptor memory 468 and queue link memory 466. Queue descriptor memory 468 may be configured to store pointers indicating the start and end of a linked list in queue link memory 466 (interpreted as virtual channel linked list). Each entry in queue link memory 466 is part of a linked list of pointers to packet numbers for representing packets stored in shared memory 440 (interpreted as virtual channel linked list) (column 10 lines 28-67). Oberman teaches in claim 8, creating and storing a packet descriptor for the packet, wherein the packet descriptor is stored in a linked list (i.e. updating an input virtual channel linked list corresponding to the input virtual channel to include the data block). As such, Examiner respectfully disagrees with the Applicant's assertion that Oberman does not recite updating an input virtual channel linked list corresponding to the input virtual channel to include the data block (see page 12 of Applicant's argument).

As such, claims 1-29 stand rejected.

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SALMAN AHMED whose telephone number is (571)272-8307. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. A./

Examiner, Art Unit 2419

/Edan Orgad/

Supervisory Patent Examiner, Art Unit 2419